Digital Logic and Design

Assignment 3

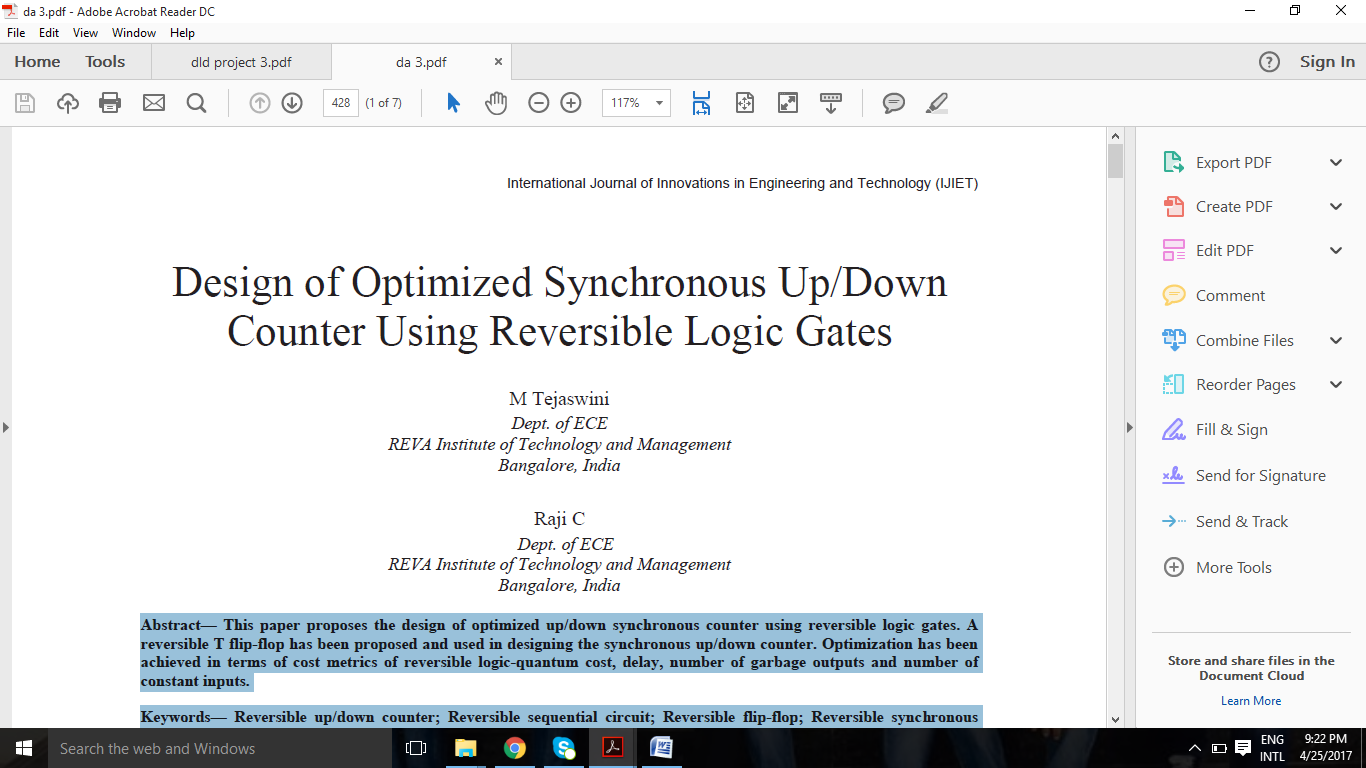
# Challenging Task

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Slot: B2

The Journal used is:-

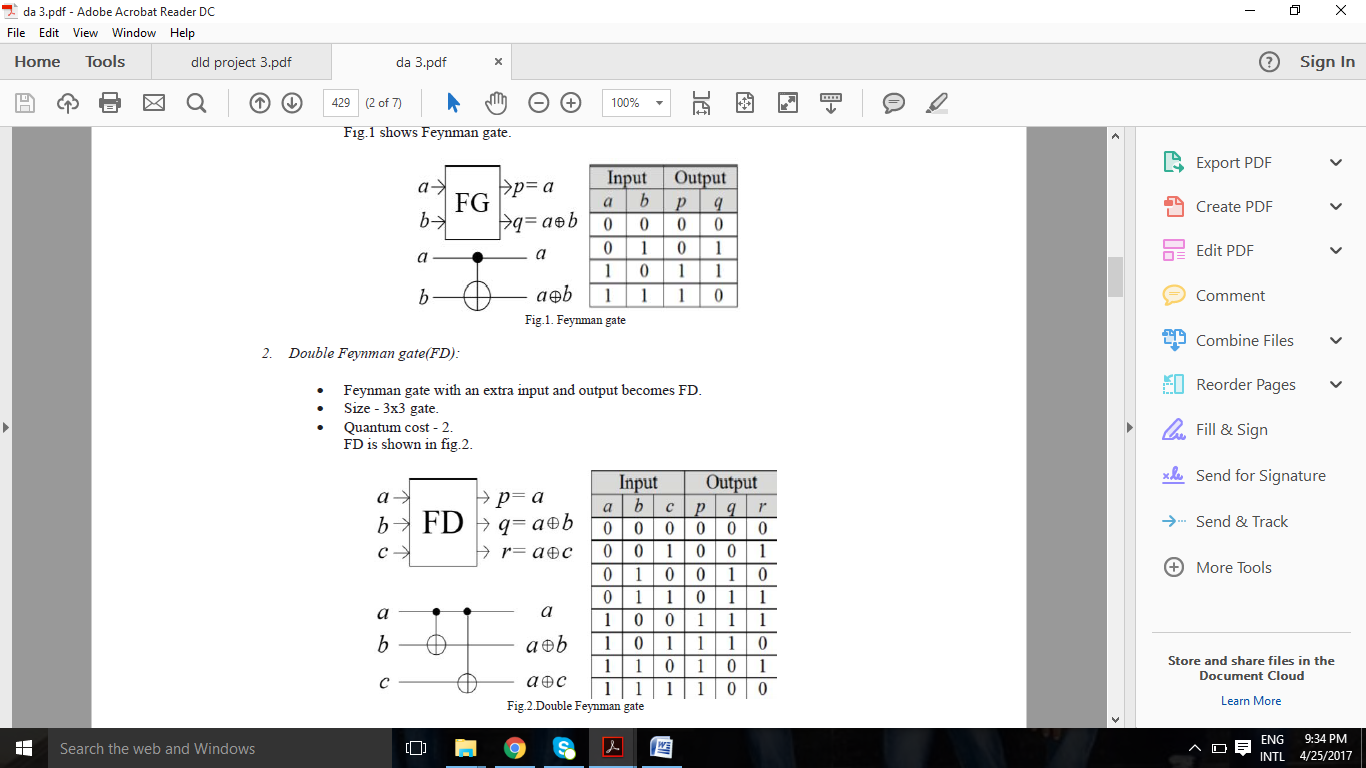


Gates used:

There are many reversible logic gates of different sizes available which are developed base on the function that has to be realized. The gates used in realizing the proposed designs are being described. Quantum representations and Truth Tables of respective gates are also mentioned.

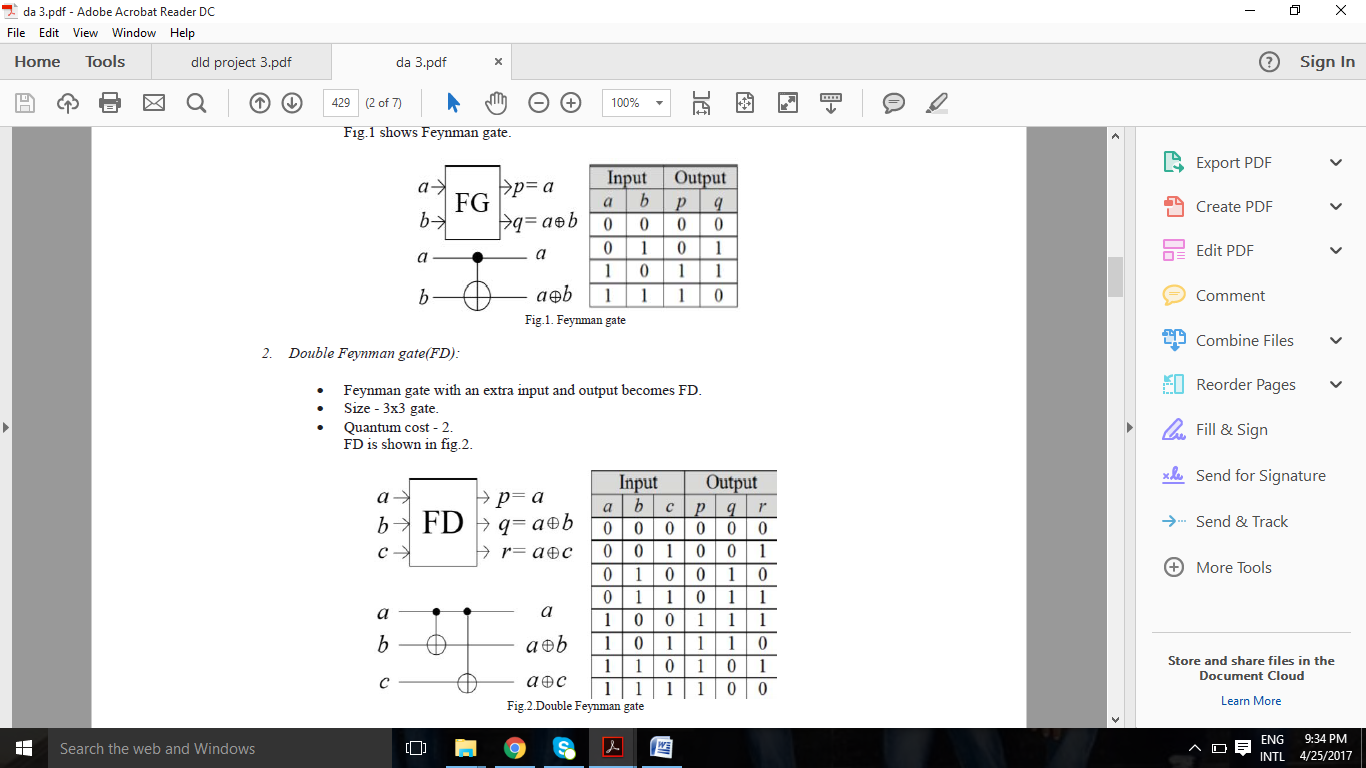
1. Feynman gates(FG)

* The basic reversible logic gate.
* Size – 2x2.
* Otherwise called as Controlled-NOT gate.
* Quantum cost is 1.
* As Fan-out is prohibited in reversible computing, Feynman gate acts as copying gate.



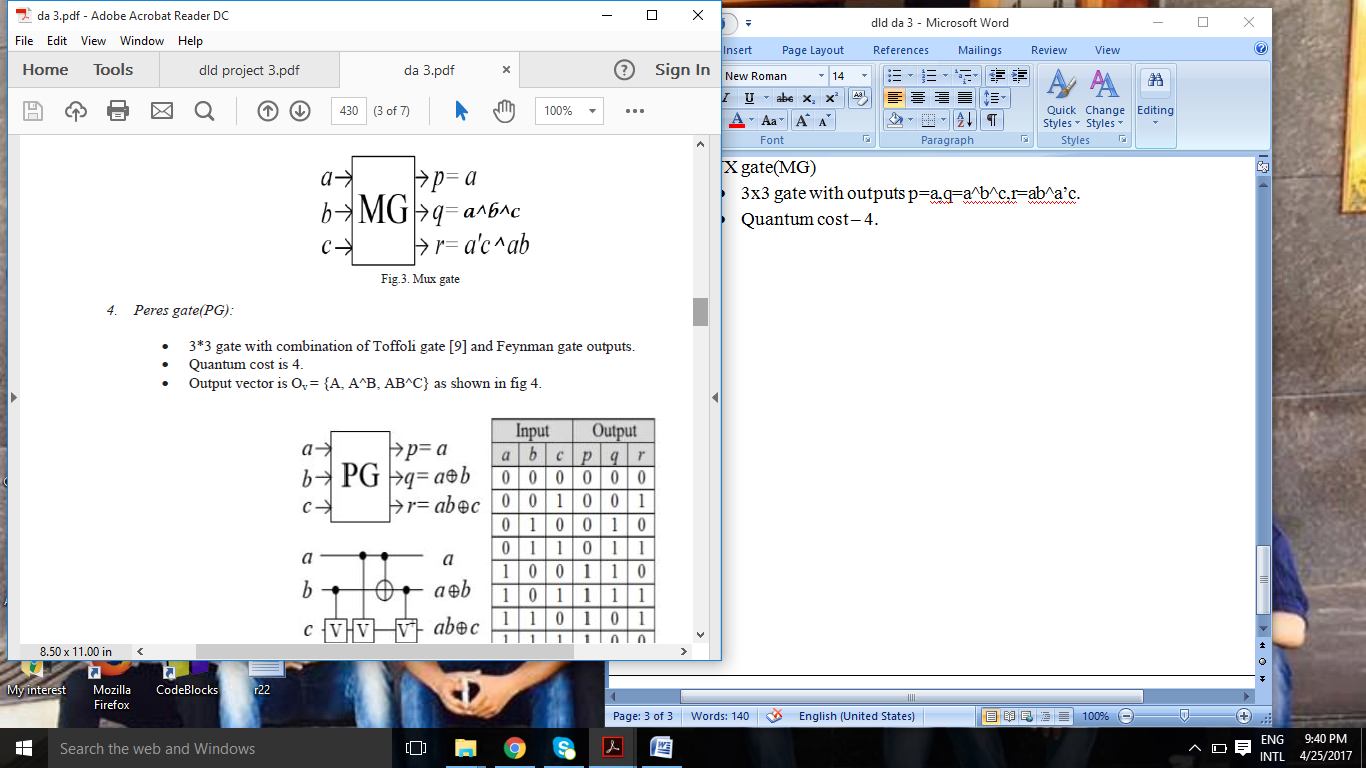
1. Double Feynman gate(FD):

* Feynman gate with an extra input and output becomes FD.
* Size – 3x3 gate.
* Quantum cost – 2.



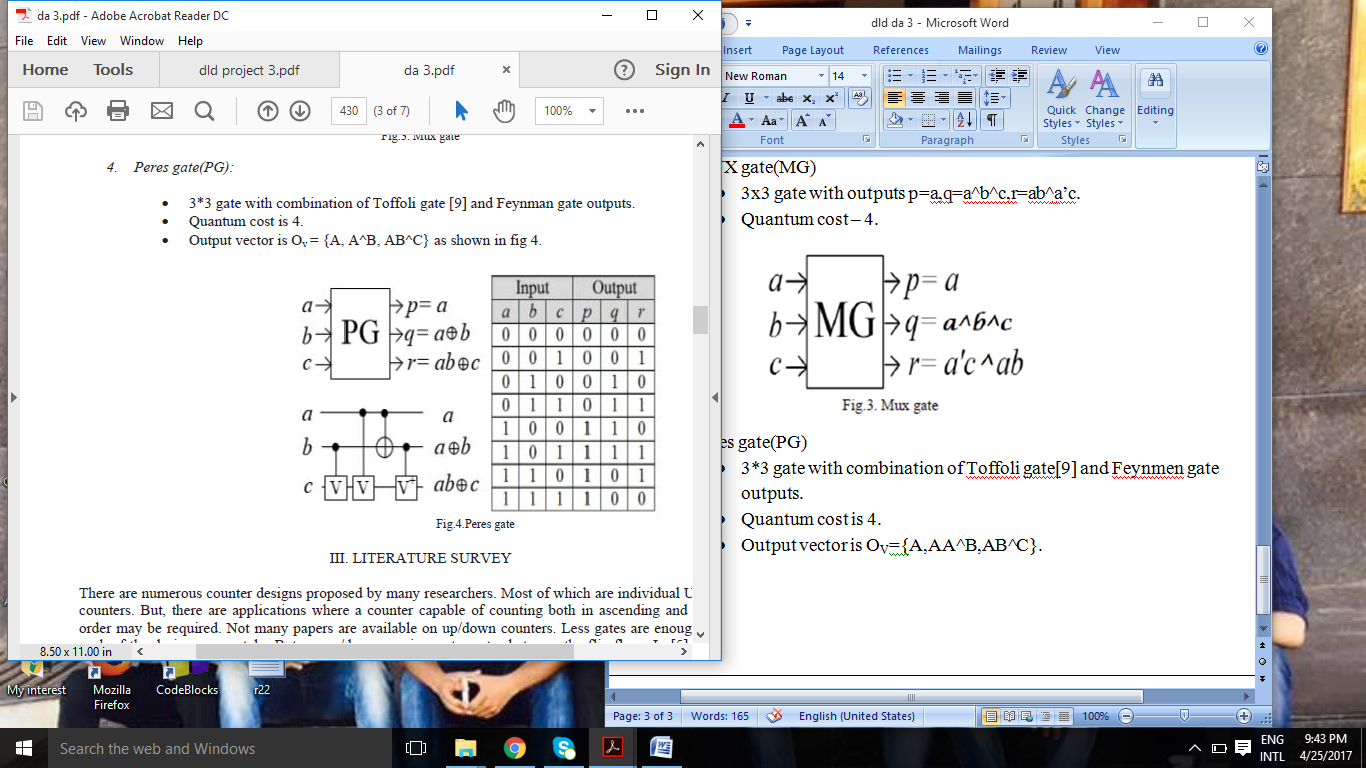
1. MUX gate(MG)

* 3x3 gate with outputs p=a,q=a^b^c,r=ab^a’c.
* Quantum cost – 4.



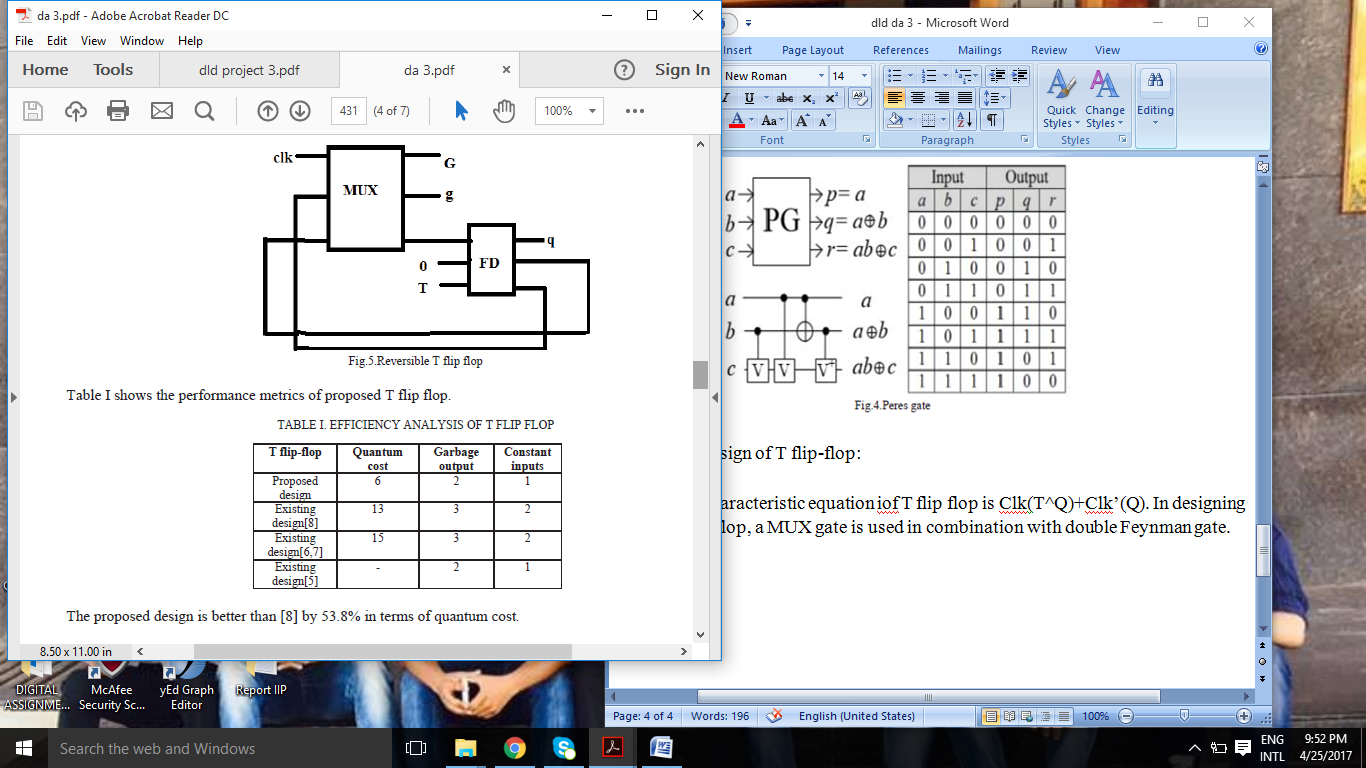
1. Peres gate(PG)

* 3\*3 gate with combination of Toffoli gate[9] and Feynmen gate outputs.
* Quantum cost is 4.
* Output vector is OV={A,AA^B,AB^C}.



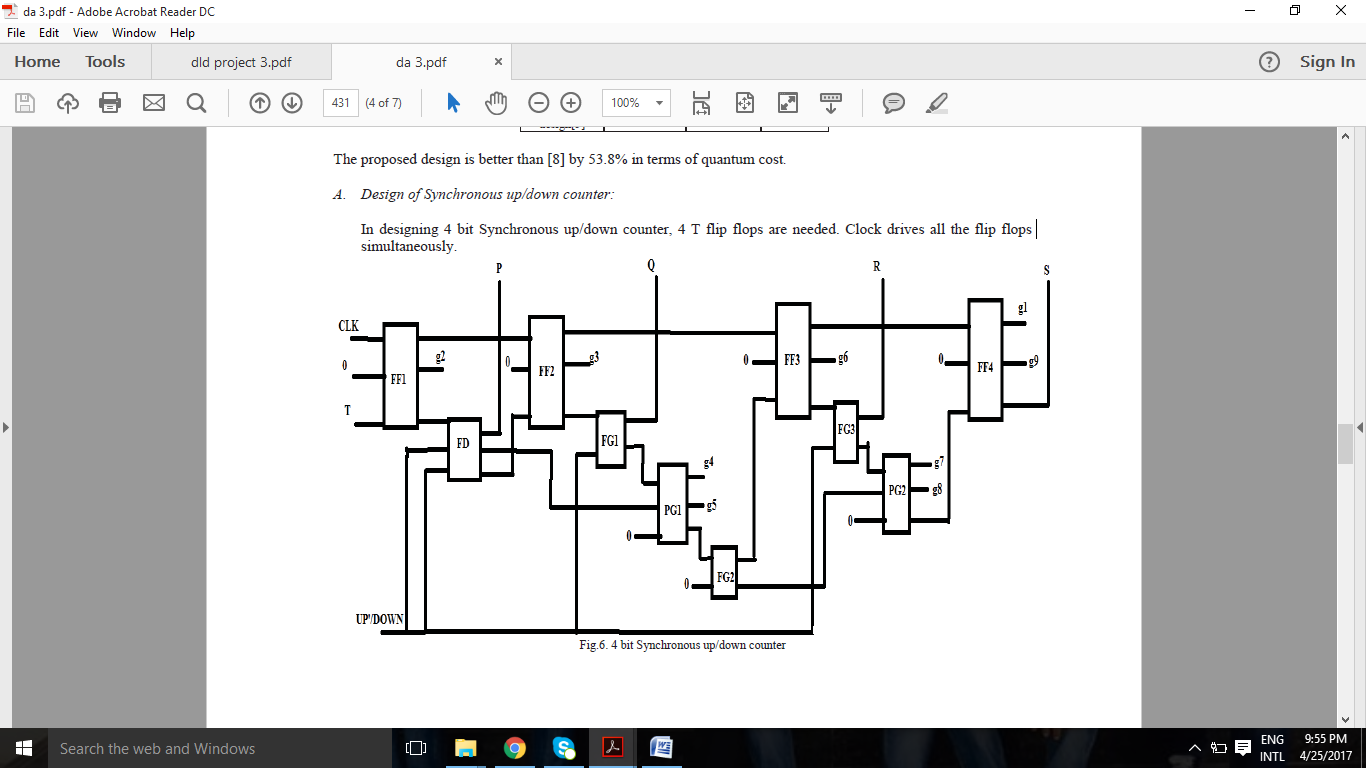
1. The design of T flip-flop:

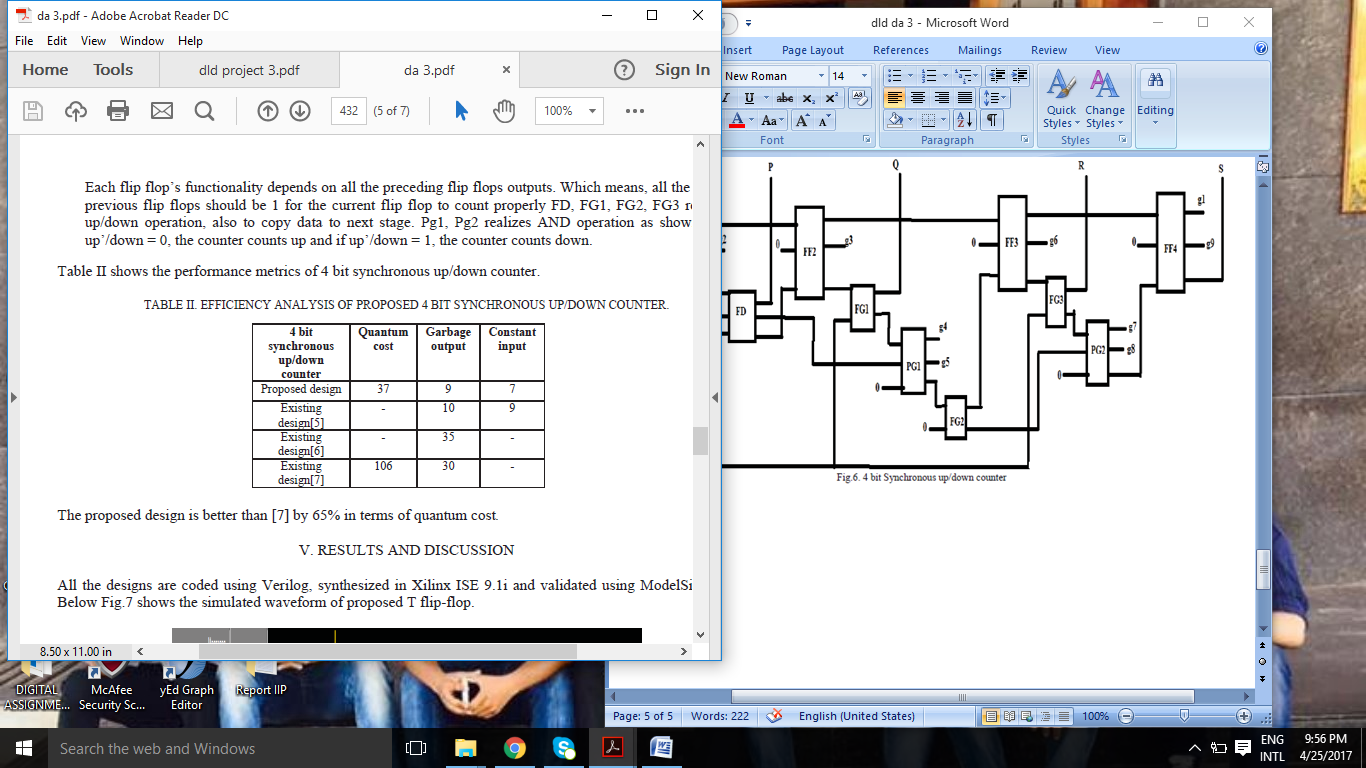
The characteristic equation iof T flip flop is Clk(T^Q)+Clk’(Q). In designing T flip flop, a MUX gate is used in combination with double Feynman gate.



1. Design of Synchronous up/down counter:

In designing 4 bit Synchronous up/down counter, 4 T flip flops are needed. Clock drives all the flip flops simultaneously.





Results:

The designs are coded using Quatarus II and validated using ModelSim Altera. The stimulated waveform of proposed in T flip-flop.

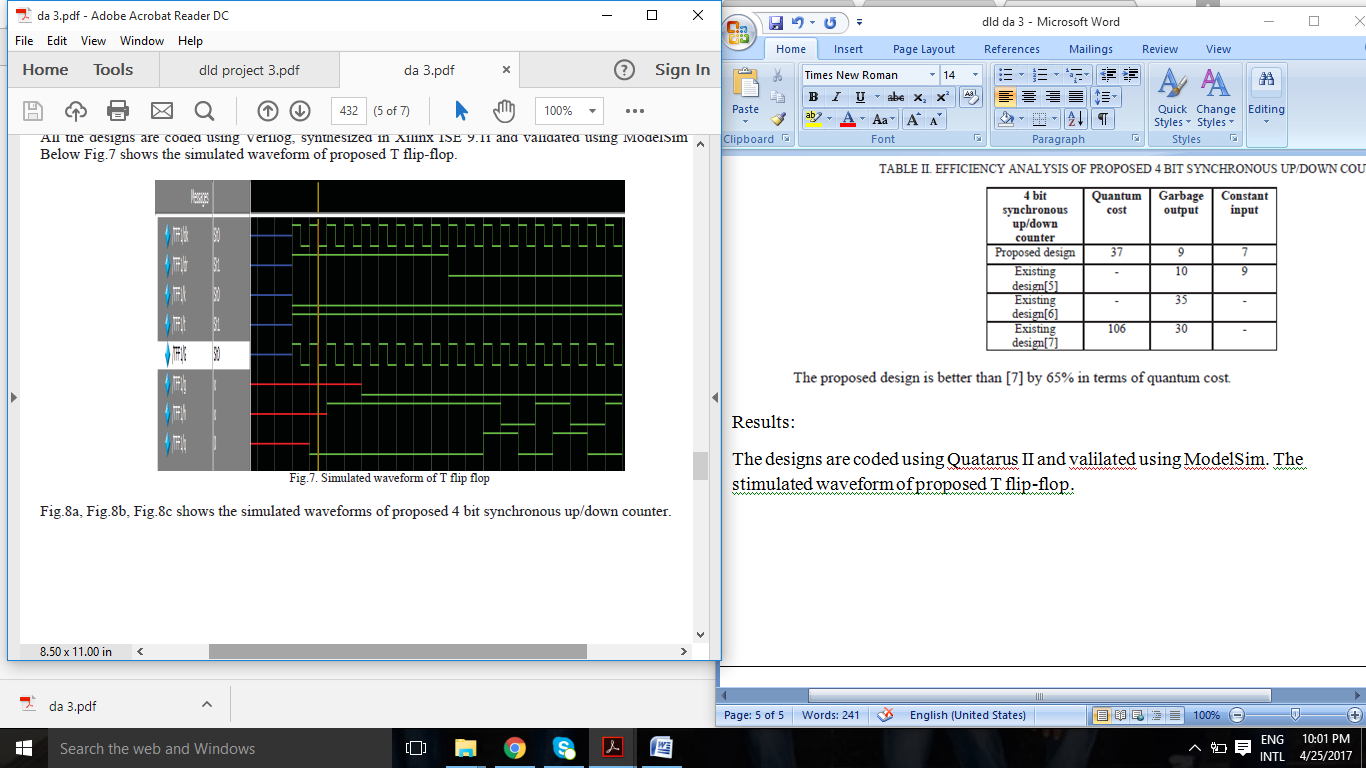


Fig: The simulated waveforms of proposed 4 bit synchronous up/down counter uisnig T flip-flop.

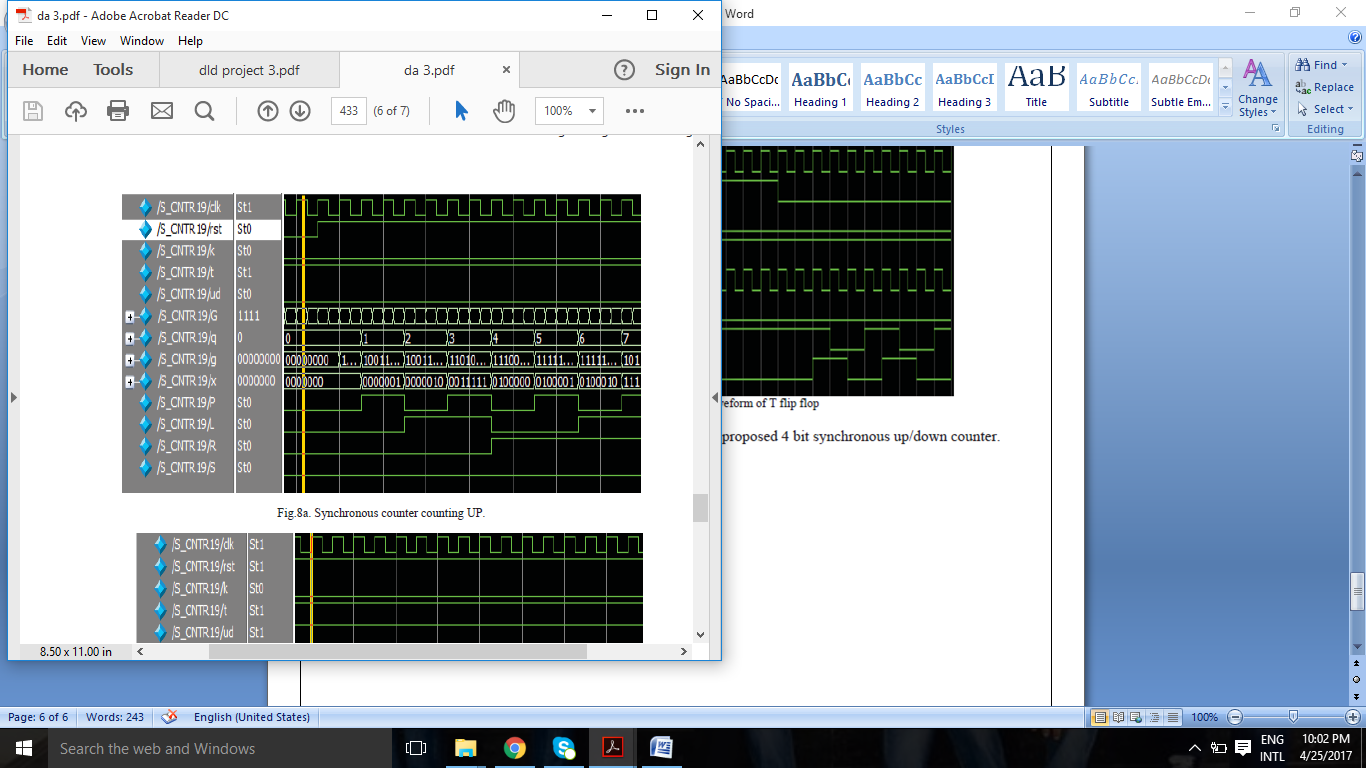


Fig: Synchronous counter counting UP

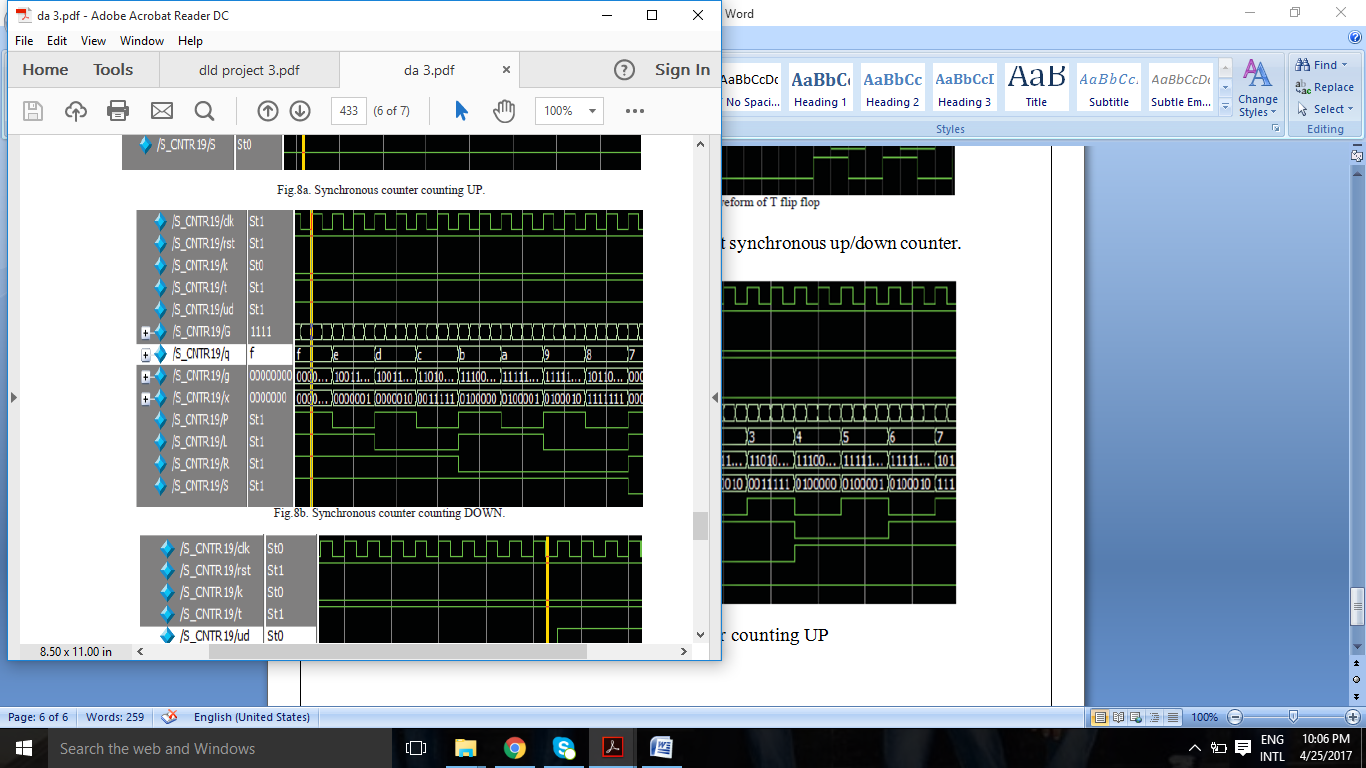


Fig: Synchronous counter counting DOWN.

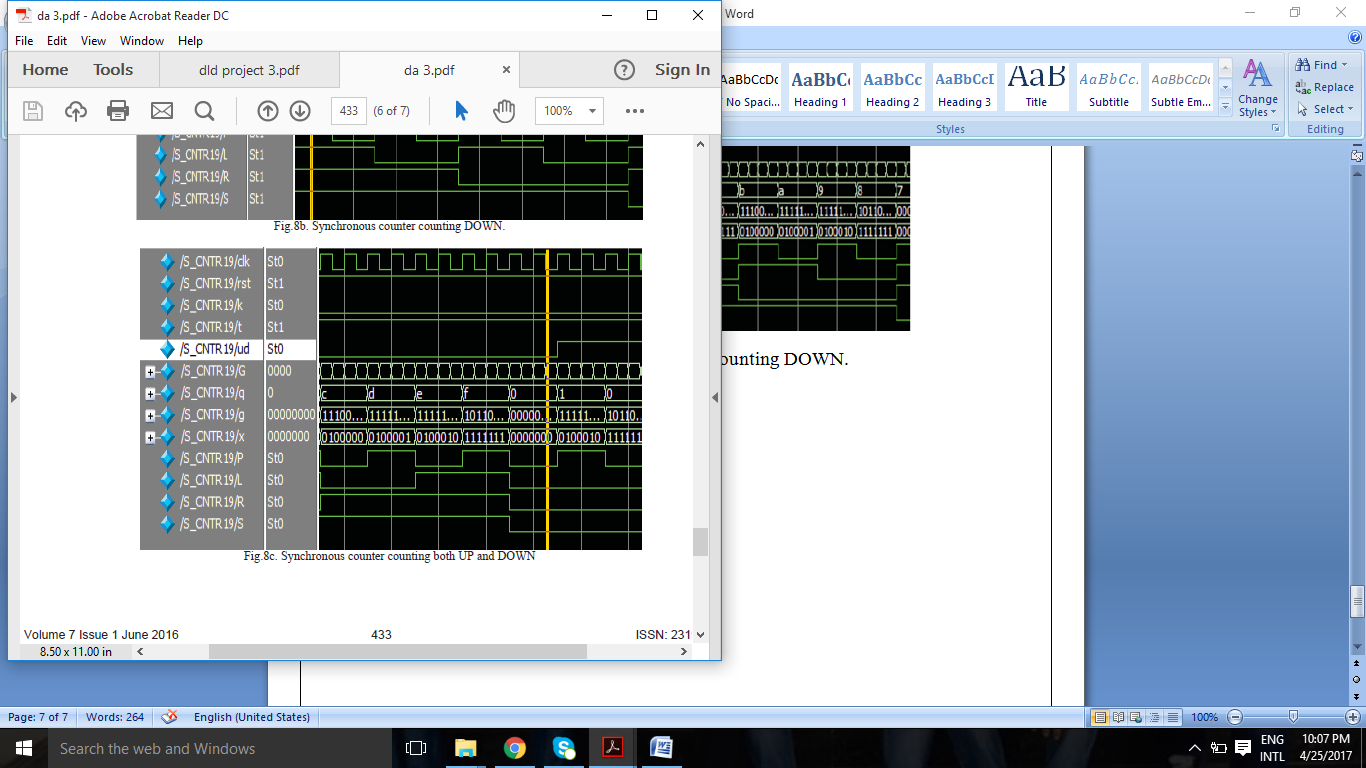
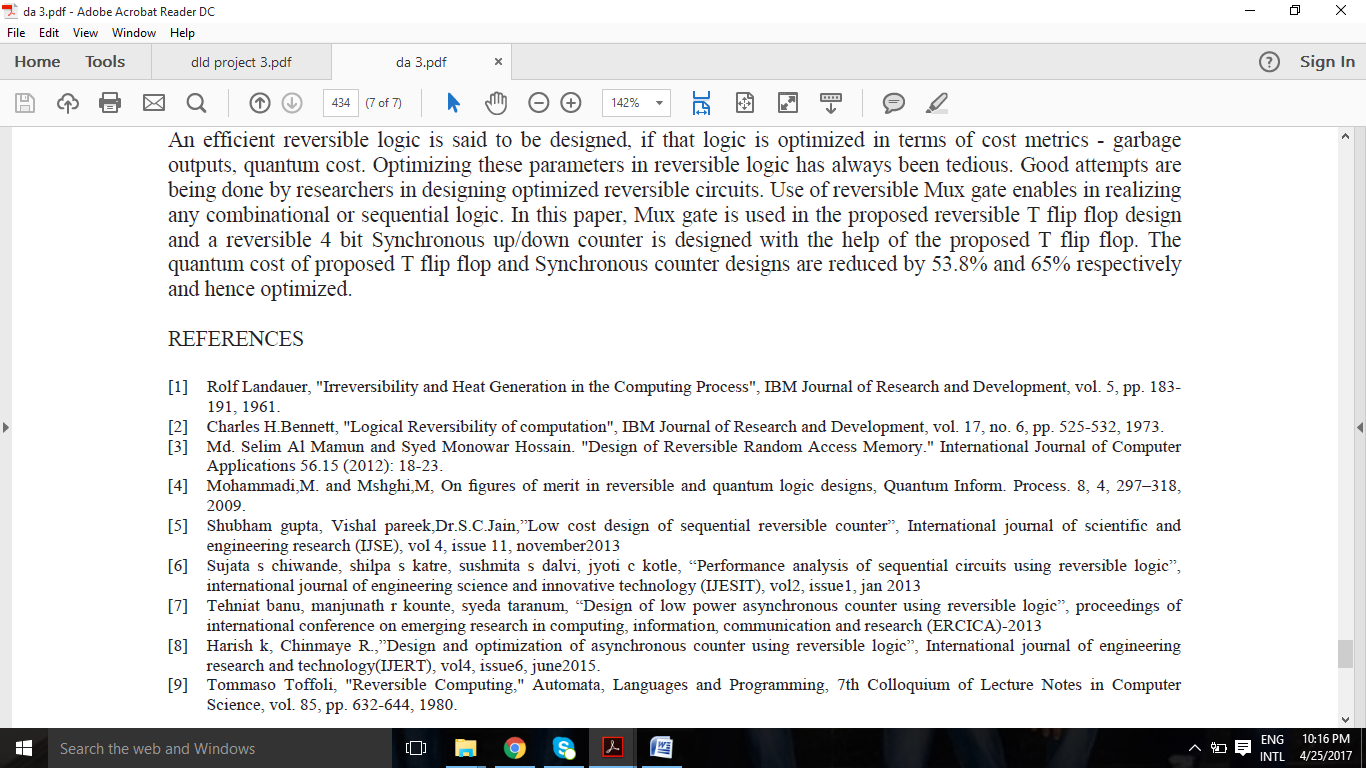


Fig: Synchronous counter counting DOWN and UP.

Conclusion:



Reference:

